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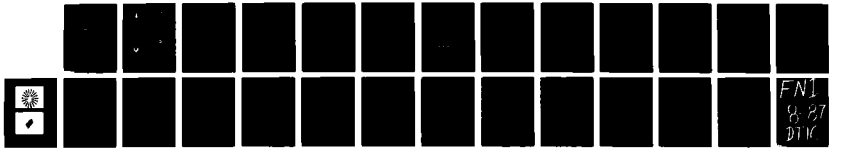

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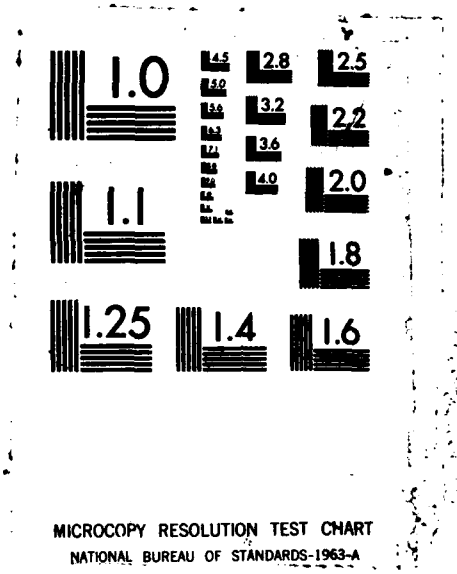
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TECHNICAL REPORT RD-RE-86-10

FAST MICROCOMPUTER CONTROL OF A MAGNETO-OPTIC SPATIAL LIGHT MODULATOR

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Research, Development, and Engineering Center

AUGUST 1986

U.S. ARMY MISSILE COMMAND
Redstone Arsenal, Alabama 35898-5000

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved
OMB No 0704-0188
Exp. Date Jun 30, 1986

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution is unlimited.
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) TR-RD-RE-86-10	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION Research Dir. Res, Dev, and Eng Ctr 6b. OFFICE SYMBOL (If applicable) AMSMI-RD-RE	7a. NAME OF MONITORING ORGANIZATION
6c. ADDRESS (City, State, and ZIP Code) Commander US Army Missile Command ATTN: AMSMI-RD-RE Redstone Arsenal, AL 35898	7b. ADDRESS (City, State, and ZIP Code)
8a. NAME OF FUNDING/SPONSORING ORGANIZATION 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State, and ZIP Code)	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT ACCESSION NO

11. TITLE (Include Security Classification)

Fast Microcomputer Control of a Magneto-Optic Spatial Light Modulator

12. PERSONAL AUTHOR(S)
D. J. Lanteigne and T. D. Hudson

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Final	FROM _____ TO _____	1986 August	

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Microcomputer control of the Litton magneto-optic spatial light modulator has been implemented in a FORTH-derived language. An image can be written to the 16,384 pixels of the device in a little over a second, and software is easily modified to meet research needs.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21 ABSTRACT SECURITY CLASSIFICATION
☒ UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT ☐ DTIC USERS	
22a. NAME OF RESPONSIBLE INDIVIDUAL	22b TELEPHONE (Include Area Code) / 22c OFFICE SYMBOL

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LIST OF ILLUSTRATIONS

I. INTRODUCTION

The practical use of coherent optical correlators for target recognition demands a spatial light modulator capable of displaying input images and filters in real time. A candidate for this role is the magneto-optic spatial light modulator manufactured by Litton and Semetex [1] . The modulator is a partially transparent array of pixels on a semiconductor chip. Each pixel is made of a magnetic film that exhibits Faraday rotation of polarized light. The sense of the rotation, either to the right or to the left, depends upon the magnetic polarity of the film, either "up" or "down". Figure 1 shows how the magnetic state of a pixel can be viewed as a binary modulation of the light amplitude passing through it. The polarity of each pixel can be controlled by means of currents driven through a grid of conductors surrounding the pixels, with the aid of an externally applied magnetic field.

The accomplishment outlined in this report is the control of a 128 x 128 pixel array light modulator by an 8085-based microcomputer programmed in the FORTH language. Litton supplied assembler software to control the device via a 6502 processor, but straight assembler code is difficult to modify for the changing needs of a laboratory situation. The FORTH language provides this flexibility, offers high level constructs such as DO loops, and supports assembler sub-routines for fast operation. In the final version of the FORTH software, an image could be written to the Litton magneto-optic spatial light modulator in 1.2 seconds at an average rate of one pixel every 73 micro-seconds.

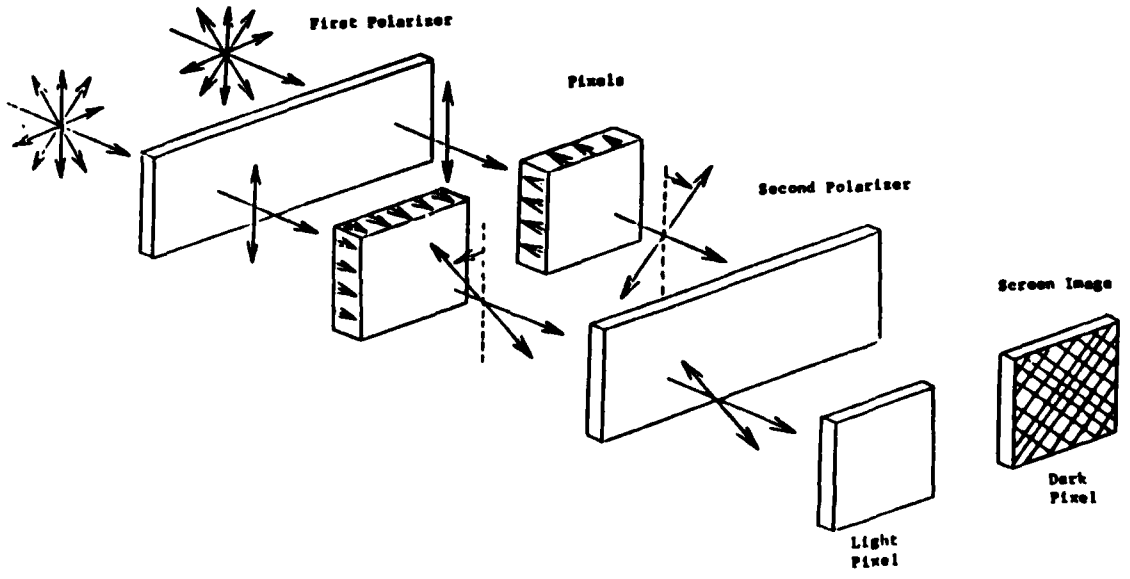

Figure 1. Optical modulation through the magneto-optic (Faraday) effect.

II. THE LITTON 128-03 SPATIAL LIGHT MODULATOR

The magneto-optic device used in this work was a Litton 128-03 LIGHT-MOD. It consists of a square array of 128 x 128 pixels on 76 μm centers. Each pixel is 58 μm x 58 μm. Conducting lines deposited on the chip form a grid between the pixels. One corner of each pixel is ion implanted so as to be especially susceptible to applied magnetic fields (see Figure 2).

In operation, currents are driven simultaneously through two orthogonal lines. At their intersection, they produce a sufficiently strong field to set the polarity of the implanted corner on the nearest pixel. Then, with the aid of an externally applied magnetic field from a coil surrounding the chip, the magnetic domain of the new state expands to cover the whole pixel. The polarization state of the light passing through the pixel is then changed accordingly [2].

The driver electronics of the light modulator serve to direct the current pulses on the chip and in the external field coil. Although some of the drive electronics are fabricated together with the magneto-optic chip, most are on an external circuit card. Although the light modulator is capable of switching one row or column at a time, the currently available driver can address only one pixel at a time [3].

A pixel is switched by sending two addresses, two timing signals, and a polarity signal to the driver board. All signal levels are TTL standard. Two seven-bit addresses serve to specify the X and Y coordinates of a pixel. A negative-going edge on line PT triggers the current pulses on the chip that

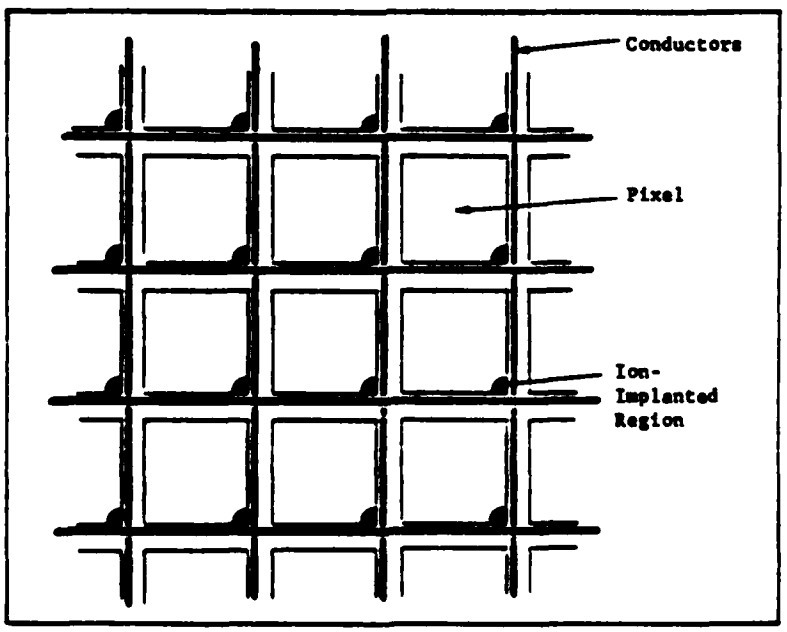

Figure 2. Pixel structure of the magneto-optic spatial light modulator.

intersect at the addressed pixel. A negative-going edge on the line PC triggers the current pulse through the field coil. The polarity signal on line SPA7 determines the direction of both chip and coil currents, so as to write or erase the pixel.

The time at which each pulse is triggered is controlled by software, but pulse widths are set by the driver board. The duration of chip current pulses triggered by edge PT are timed by a one-shot to one microsecond. Likewise, the coil current pulse is set to last for about 0.6 millisecond. A shorter coil pulse is not practical because of the long inductive time constant of the coil.

III. SOFTWARE CONTROL OF THE LITTON DEVICE

Control of the Litton device was achieved with a Zenith Z-100 microcomputer using an 8085A microprocessor. The software was developed in a dialect of the FORTH language (4th, by United Controls Corporation) [5]. FORTH-based languages are well-suited to device control, as they can incorporate fast assembly-language routines into code, as well as supporting high-level programming tools [4].

The Litton device was operated in the bias-assist mode, which means that chip and coil currents were active simultaneously, so as to minimize power dissipation in the chip. In the bias-assist mode, X and Y pixel addresses must be set at the proper ports of the driver card, and then the SPA7 polarity bit, which will determine current flow direction and thus the final state of the pixel. Coil current is then triggered by the falling edge of PC. After allowing 225 μsec for the current in the field coil to build up against inductive delay, PT triggers the chip currents that effect the pixel write or erase operation.

The first routine to implement the bias-assist mode was called "1D128" (see appendix). 1D128 implements a doubly-nested 128 x 128 DO loop. The loop counters I and J represent the pixel addresses, and are both placed on the microprocessor stack. (FORTH uses a stack-oriented, RPN arithmetic). The counters are also used to calculate the computer memory address that contains the bit representing that pixel, and a bit mask to sift that one bit out of its memory address. These values are passed on the stack to assembly language routine 1N128, which determines the polarity of the pixel, and activates PC and SPA7 simultaneously. A delay loop is run for 225 μsec (COIL.RISE.DELAY), and then the X and Y values are output to ports that connect to the driver card address lines. PT is then activated, and control returns to 1D128 to set up the parameters for the next pixel and start again after the coil current has decayed. A schematic of the pulse timing is shown in Figure 3.

1D128 writes an image to the 16,384 pixels of the device in 48 seconds. The algorithm is slow because the delay between pixels is set by the near-millisecond time constant of the coil current and the unexpectedly high overhead time associated with doubly-nested DO loops. A faster approach is to erase all pixels under the cover of one long coil current pulse, then reverse the polarity of the coil current, and write to all required pixels. In this fashion, the delay between addressing of consecutive pixels is limited only by the speed of the microprocessor in loading the pixels of the bitmapped image and sending them out with proper addresses and timing signals. The coil current can be prolonged indefinitely by repeatedly retriggering the one-shot that shapes the pulse.

The faster algorithm for writing to the Litton device is shown in the appendix. The word LITTON first invokes the word ERA128, which performs a 128 step DO loop, each time invoking the assembly language routine ERASEROW. ERASEROW, in turn, sets up a coil pulse of erase polarity and triggers chip currents to sequentially erase all the pixels in a row, while periodically retriggering the coil current. After ERA128 is completed, the whole device has been erased. In the same fashion, WRITE128 repeatedly invokes WRITEROW.

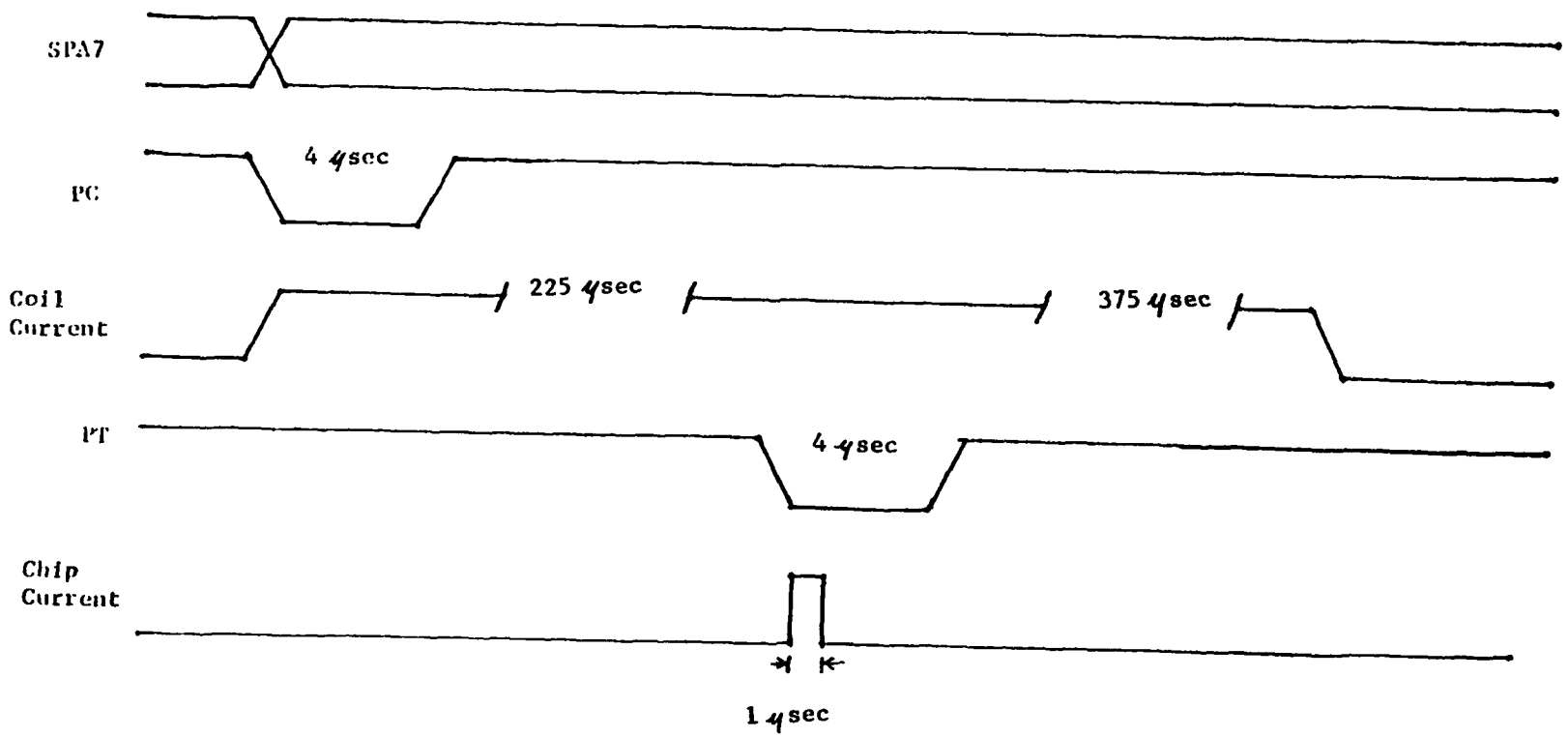

Figure 3: Pulse Timing Diagram of 1D128 Algorithm.

WRITEROW has a logic similar to ERASEROW, except that the bitmap location corresponding to each pixel must be tested to see if a PT signal is required for a write at that spot. On each row, only the "on" pixels are written to, while the coil current is repeatedly refreshed by pulsing PC low. Pulse timing is shown in Figure 4. A complete erase and write operation takes 1.2 seconds.

If one wishes to study these routines, it is helpful to know that the pixel X address is mapped to an 8-bit port labelled X.CTL.PORT, as the Y address is mapped to Y.CTL.PORT. A single port called either COIL.CTL.PORT or TRIGGER.CTL.PORT maps SPA7 (the least significant or zeroth bit), PT (the first bit), and PC (the second bit). The other five bits of the port are unused. All assembler mnemonics are based on Intel standard, but the operands precede the mnemonics, and FORTH conditional constructs such as BEGIN ... ENDZ (end on zero) are used.

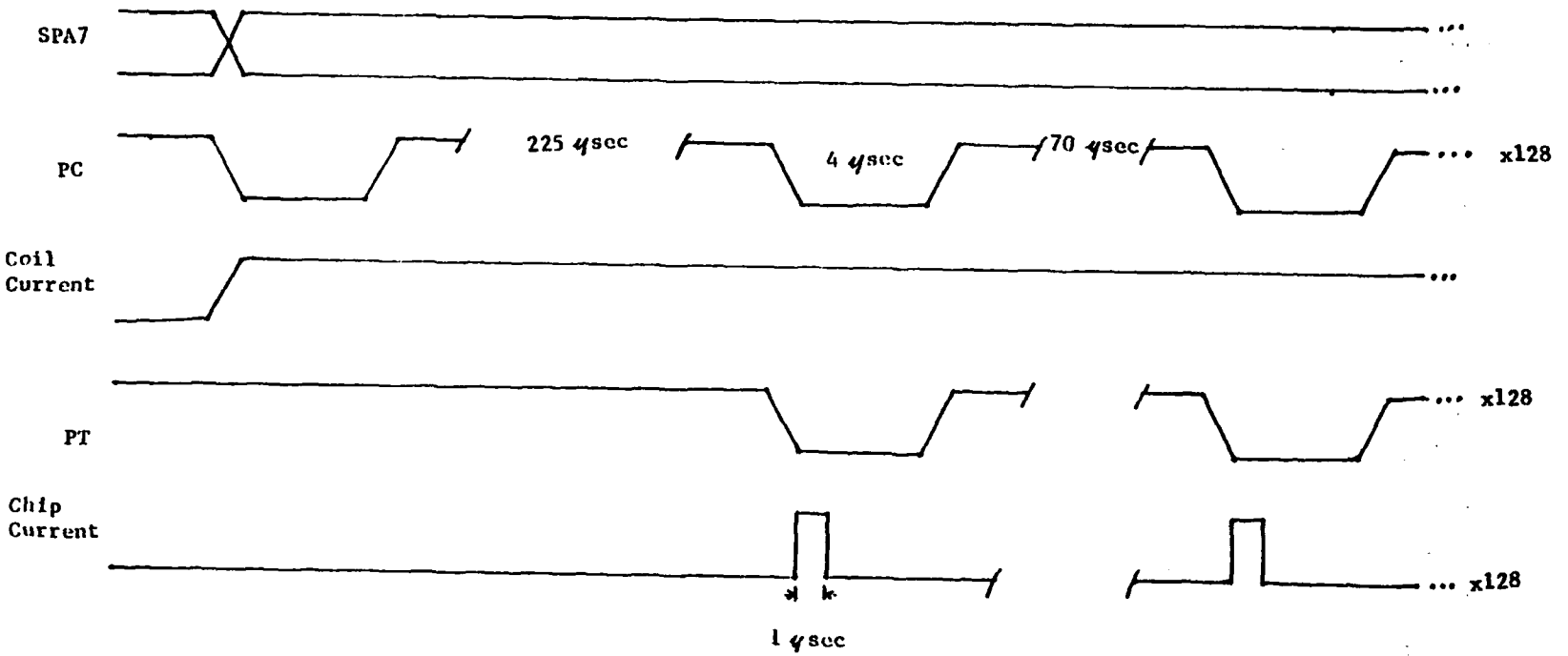

Figure 4: Pulse Timing of LITTON Algorithm.

IV. CONCLUSION

Figure 5 shows two images written to the Litton device using the FORTH word LITTON. The combination erase/write operation takes 1.2 seconds. (As is usual for this device, some pixels are switched on randomly, due to varying magnetic susceptibility across the face of the chip). This is satisfactory for laboratory work, but is probably near the lower limit possible for microprocessor control of the present driver electronics. The sequential fetching of data, calculation, and output of addresses and timing signals takes far longer than the approximately 1 microsecond needed to switch a pixel. Increasing the writing speed to video frame rates and beyond will require simultaneous, parallel addressing of a whole row of pixels, perhaps supported by some form of direct memory access that bypasses the microprocessor. However, in lieu of such special purpose hardware, FORTH based software will continue to provide a suitable combination of speed, flexibility, and ease of modification for changing laboratory needs.

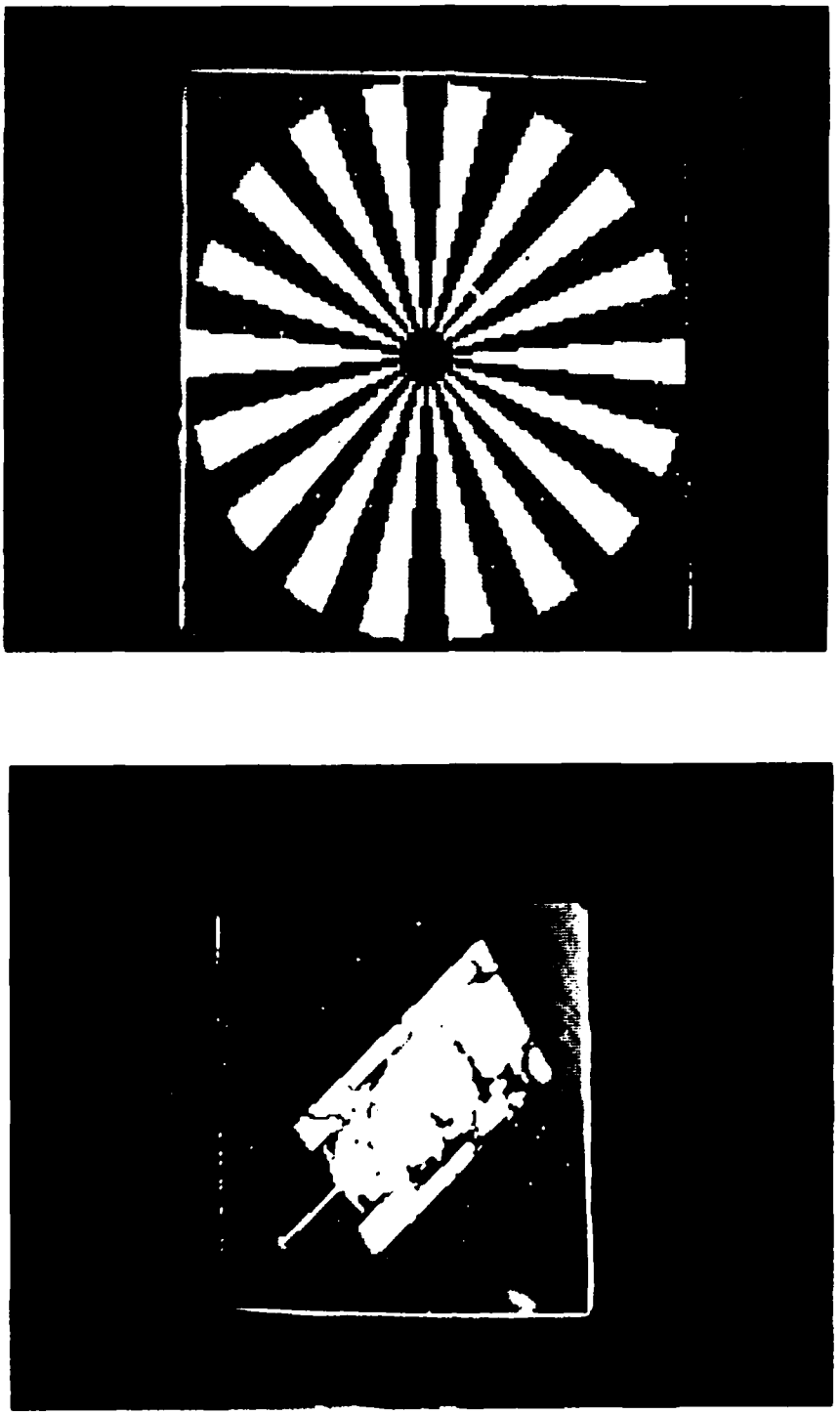

Figure 5. Images displayed on the Litton magneto-optic spatial light modulator.

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5. Jennings, R. S., The 4th Language Reference Manual, (United Controls Corporation, Huntsville, AL).

APPENDIX

APPENDIX

1D128

```
1ND128.4TH

DATA[ 1 ] COIL.FALL.DELAY
DATA[ 61  ] COIL.RISE.DELAY

CODE 1N128 ( X*256+Y, bitmask,bitmapADDR--)
  H POP,    ( get bitmapADDR into regHL)                          ( 10T)
  D POP,    ( get bitmask into  regE, regD unaffected)            ( 10T)
  A E MOV,                                                        (  4T)
  M ANA,                                                          (  7T)
  IFNZ A PIXEL.ON MVI, THEN                                       ( 10T)
  D A MOV,                                                        (  4T)
  PC.LEADING.EDGE ORI, TRIGGER.CTL.PORT OUT,                      ( 17T)
  A D MOV,                                                        (  4T)
  PC.TRAILING.EDGE ORI, TRIGGER.CTL.PORT OUT,                     ( 17T)
  '' COIL.RISE.DELAY LHLD, BEGIN                                  ( 16T)
      L DCR, ENDZ                                                 ( 14T)
  H POP,    ( Y into regL, X into regH)                           ( 10T)
  A L MOV, Y.CTL.PORT OUT,                                        ( 14T)
  A H MOV, X.CTL.PORT OUT,                                        ( 14T)
  A D MOV,  ( restore SPA7 bit)                                   (  4T)
  PT.LEADING.EDGE ORI, TRIGGER.CTL.PORT OUT,                      ( 17T)
  A D MOV,                                                        (  4T)
  PT.TRAILING.EDGE ORI, TRIGGER.CTL.PORT OUT,                     ( 17T)
  '' COIL.FALL.DELAY LHLD, BEGIN                                  ( 16T)
      NOP, NOP, NOP,                                              ( 12T)
      L DCR, ENDZ                                                 ( 14T)
;

: 1D128 ( display bitmap to L-128)
  127 0 DO
    127 0 DO
      I SHL8 J OR ( leave X*256+Y on stack)
      I 8 /MOD DROP ORTABLE + B@ ( leave bitmask on stack)
      I J CELLADR 8 / BITMAP +   ( leave address on stack)
          1N128
    LOOP
  LOOP
;


00000000B CONST PIXEL.OFF
00000001B CONST PIXEL.ON
11111100B CONST PT.LEADING.EDGE
11111110B CONST PT.TRAILING.EDGE
11111010B CONST PC.LEADING.EDGE
11111110B CONST PC.TRAILING.EDGE
```

LITTON.4TH

```
" ERASEMAP.4TH" LOAD
" WRITEMAP.4TH" LOAD

: LITTON   ERA128 WRITE128 ;
```

ERASEMAP.4TH

```
00000000B CONST LEADING.EDGE
00000110B CONST TRAILING.EDGE

CODE ERASEROW
   H B MOV, L C MOV, '' 4TH.PROGRAM.COUNTER SHLD.
   B  POP.  ( PLACES I,  THE Y-COORDINATE INTO REG C )    ( 10T)
   B 127 MVI,                                             (  7T)
   A PC.LEADING.EDGE MVI, TRIGGER.CTL.PORT OUT,           ( 17T)
   A PC.TRAILING.EDGE MVI, TRIGGER.CTL.PORT OUT,          ( 17T)
   '' COIL.RISE.DELAY LHLD, BEGIN                         ( 16T)
      L DCR, ENDZ                                         ( 14T)
BEGIN
   A C MOV, Y.CTL.PORT OUT,                               ( 14T)
   A B MOV, X.CTL.PORT OUT,                               ( 14T)
   A LEADING.EDGE MVI, COIL.CTL.PORT OUT,                 ( 17T)
   A TRAILING.EDGE MVI, COIL.CTL.PORT OUT,                ( 17T)
   B DCR, ENDZ                                            ( 14T)
'' 4TH.PROGRAM.COUNTER LHLD, B H MOV, C L MOV,
;

: ERA128
    127 0 DO
            I
            ERASEROW
            LOOP
;
```

```
WRITEMAP.4TH

2 BLOCK BITMAPADDR
11111001B CONST PC.PT.LEAD
11111111B CONST TRAILING.WRITE
11111011B CONST PC.LEAD.WRITE

CODE WRITEROW
   H B MOV, L C MOV, '' 4TH.PROGRAM.COUNTER SHLD,
   C 0 MVI,                                                    ( 7T)
   D  POP,  (  PLACES  I,  THE Y-COORDINATE  INTO  REG  E,  REG  D
UNAFFECTED)                                                    ( 10T)
   A E MOV, Y.CTL.PORT OUT,                                    ( 14T)
   A PC.LEAD.WRITE MVI, TRIGGER.CTL.PORT OUT,                  ( 17T)
   A TRAILING.WRITE MVI, TRIGGER.CTL.PORT OUT,                 ( 17T)
   '' COIL.RISE.DELAY LHLD, BEGIN                              ( 16T)
      L DCR, ENDZ                                              ( 14T)
BEGIN
  '' BITMAPADDR LHLD,                                          ( 16T)
  A L MOV, 1 ADI,                                              ( 11T)
  L A MOV,                                                     ( 4T)
  IFC
  A H MOV, 1 ADI, H A MOV,                                     ( 15T)
  THEN
    D H MOV, E L MOV,                                          ( 8T)
    '' BITMAPADDR SHLD,                                        ( 16T)
B 0 MVI,                                                       ( 7T)
BEGIN
  A B MOV, 0 SUI,                                              ( 11T)
IFZ
  D LDAX,                                                      ( 7T)
ELSE
  A L MOV,                                                     ( 4T)
THEN
  RAL,                                                         ( 4T)
  L A MOV,                                                     ( 4T)
IFC
  A C MOV,                                                     ( 4T)
  RLC, RLC, RLC,                                               ( 12T)
  B ADD, X.CTL.PORT OUT,                                       ( 14T)
  A PC.PT.LEAD MVI, TRIGGER.CTL.PORT OUT,                      ( 17T)
  A TRAILING.WRITE MVI, TRIGGER.CTL.PORT OUT,                  ( 17T)
ELSE
  A PC.LEAD.WRITE MVI, TRIGGER.CTL.PORT OUT,                   ( 17T)
  A TRAILING.WRITE MVI, TRIGGER.CTL.PORT OUT,                  ( 17T)
THEN
   B INR, A B MOV, 8 SUI, ENDZ                                 ( 21T)
   C INR, A C MOV, 16 SUI, ENDZ                                ( 21T)

'' 4TH.PROGRAM.COUNTER LHLD, B H MOV, C L MOV,
;

: WRITE128
   BITMAP 1- BITMAPADDR !
   127 0 DO
         I
         WRITEROW
         LOOP
;
```

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